CLAIM LISTING

This listing of the claims, if entered, replaces all prior versions of the claims.

1 (Previously Presented) A method for implementing a circuit representing a complex polynomial equation in a hardware description language comprising:

implementing a serial circuit representing the complex polynomial equation in a software program; wherein implementing the serial circuit includes

storing a plurality of ASCII strings in each of a plurality of storage elements, wherein the plurality of ASCII strings represent a plurality of initial values of the serial circuit,

storing one or more ASCII strings in each of one or more data structures wherein the one or more ASCII strings represent one or more mathematical operations in the serial circuit, and

simulating the serial circuit to produce a plurality of parallel equations, wherein simulating the serial circuit includes

simulating the serial circuit for a plurality of cycles as required to produce one output represented by the plurality of parallel equations.

2. (Original) The method as recited in Claim 1, wherein storing the one or more ASCII strings comprises:

storing an ASCII string "XOR" for each addition operation in the serial circuit; and

storing an ASCII string "AND" for each multiplication operation in the serial circuit.

3. (Original) The method as recited in Claim 1, wherein the complex polynomial equation is a Bose-Chaudhuri-Hocquenghem (BCH) code utilized in forward error correction circuitry.

4. (Previously Presented) The method as recited in Claim 1, further comprising:

writing the plurality of parallel equations to an output file;

removing initial register values from each of the parallel equations;

adding a feedback value to each of the parallel equations; and

merging the parallel equations into a hardware description language (HDL) code file.

5. (Original) The method as recited in Claim 4, further comprising:
manufacturing an application specific integrated circuit from the HDL code file.

6. (Canceled)

7. (Previously Presented) A method for implementing a circuit representing a complex polynomial equation in an ASIC (Application Specific Integrated Circuit) comprising:
producing one or more parallel equations in a hardware description language, wherein the producing comprises simulating a serial circuit; and
merging the one or more parallel equations into a hardware description language implementation of a Galois Field circuit.

8. (Previously Presented) The method as recited in Claim 7, wherein producing the one or more parallel equations comprises:
implementing the serial circuit representing the complex polynomial equation in a software program; and
simulating the serial circuit to produce the one or more parallel equations.

9. (Original) The method as recited in Claim 8, wherein implementing the serial circuit comprises:
storing a plurality of ASCII strings in each of a plurality of storage elements, wherein the plurality of ASCII strings represent a plurality of initial values of the serial circuit; and
storing one or more ASCII strings in each of one or more data structures wherein the one or more ASCII strings represent one or more mathematical operations in the serial circuit.

10. (Original) The method as recited in Claim 9, wherein storing the one or more ASCII strings in each of one or more data structures comprises:
storing an ASCII string "XOR" for each addition operation the serial circuit; and
storing an ASCII string "AND" for each multiplication operation in the serial circuit.

11. (Original) The method as recited in Claim 8, wherein simulating the serial circuit comprises:

executing the serial circuit for a plurality of cycles as required to produce one output represented by the plurality of parallel equations.

12. (Original) The method as recited in Claim 7, further comprising:

synthesizing the hardware description language description implementation into a gate level implementation; and

manufacturing the ASIC from the gate level implementation.

13. (Original) The method as recited in Claim 12, further comprising:

simulating the gate level implementation to verify accurate design implementation.

14. (Original) The method as recited in Claim 7, wherein the complex polynomial equation is a Bose-Chaudhuri-Hocquenghem (BCH) code utilized in forward error correction circuitry.

15. (Original) The method as recited in Claim 7, wherein merging the one or more parallel equations into a hardware description language implementation of a Galois Field circuit comprises:

removing initial register values from each of the parallel equations; and

adding a feedback value to each of the parallel equations.

16. (Previously Presented) An apparatus for implementing complex polynomial equation mathematics in a hardware description language comprising:

means for implementing a serial circuit representing the complex polynomial equation in a software program; wherein the means for implementing the serial circuit includes

means for storing a plurality of ASCII strings in each of a plurality of storage elements, wherein the plurality of ASCII strings represent a plurality of initial values of the serial circuit,

means for storing one or more ASCII strings in each of one or more data structures wherein the one or more ASCII strings represent one or more mathematical operations in the serial circuit, and

means for simulating the serial circuit to produce a plurality of parallel equations, wherein the means for simulating the serial circuit includes

means for simulating the serial circuit for a plurality of cycles as required to produce one output represented by the plurality of parallel equations.

17. (Original) The apparatus as recited in Claim 16, wherein the means for storing one or more ASCII strings in each of the one or more data structures comprises:

means for storing an ASCII string "XOR" for each addition operation in the serial circuit; and

means for storing an ASCII string "AND" for each multiplication operation in the serial circuit.

18. (Original) The apparatus as recited in Claim 16, wherein the complex polynomial equation is a Bose-Chaudhuri-Hocquenghem (BCH) code utilized in forward error correction circuitry.

19. (Original) An apparatus for implementing a circuit representing a complex polynomial equation in an ASIC (Application Specific Integrated Circuit) comprising:

means for producing one or more parallel equations in a hardware description language, wherein the means for producing the one or more parallel equations comprises:

means for implementing a serial circuit representing the complex polynomial equation in a software program, and

means for simulating the serial circuit to produce the one or more parallel equations;

means for merging the one or more parallel equations into a hardware description language implementation of a Galois Field circuit;

means for synthesizing the hardware description language description implementation into a gate level implementation; and

means for manufacturing the ASIC from the gate level implementation.

20. (Currently Amended) The apparatus as recited in Claim 19, wherein the means for implementing the serial circuit comprises:

means for storing a plurality of ASCII strings in each of a plurality of storage elements, wherein the plurality of ASCII strings represent a plurality of initial values of the serial circuit; and

<u>means for</u> storing one or more ASCII strings in each of one or more data structures wherein the one or more ASCII strings represent one or more mathematical operations in the serial circuit.

21. (Original) The apparatus as recited in Claim 20, wherein the means for storing the one or more ASCII strings in each of the one or more data structures comprises:

means for storing an ASCII string "XOR" for each addition operation in the serial circuit; and

means for storing an ASCII string "AND" for each multiplication operation in the serial circuit.

22. (Original) The apparatus as recited in Claim 19, wherein the means for simulating the serial circuit to produce parallel equations comprises:

means for executing the serial circuit for a plurality of cycles as required to produce one output represented by the plurality of parallel equations.

23. (Original) The apparatus as recited in Claim 19, wherein the complex polynomial equation is a Bose-Chaudhuri-Hocquenghem (BCH) code utilized in forward error correction circuitry.

24. (Original) The apparatus as recited in Claim 19, wherein the means for merging the one or more parallel equations into a hardware description language implementation of a Galois Field circuit comprises:

means for removing initial register values from each of the parallel equations; and

means for adding a feedback value to each of the parallel equations.

25. (Original) The apparatus as recited in Claim 19, further comprising:

means for simulating the gate level implementation to verify accurate design implementation.

26. (Previously Presented) An apparatus for performing Galois field decoding comprising:
a receive line section module for receiving and aligning a SONET signal;
a Forward Error Correction (FEC) decoder coupled to the receive line section module, the FEC decoder for decoding FEC check bits in the SONET signal, wherein
the FEC decoder comprises a first circuit that implements one or more parallel equations, and
the one or more parallel equations are generated by simulating a serial circuit; and
a receive demultiplexer coupled to the FEC decoder, the receive demultiplexer for demultiplexing the SONET signal into a plurality of SONET datastreams.

27. (Original) The apparatus as recited in Claim 26, wherein the FEC decoder comprises:
a circuit representing a complex polynomial equation made by the method of:
producing one or more parallel equations in a hardware description language; and
merging the one or more parallel equations into a hardware description language implementation of a Galois Field circuit.

28. (Previously Presented) The apparatus as recited in Claim 27, wherein producing the one or more parallel equations comprises:
implementing the serial circuit representing the complex polynomial equation in a software program; and
simulating the serial circuit to produce the one or more parallel equations.

29. (Original) The apparatus as recited in Claim 28, wherein implementing the serial circuit comprises:
storing a plurality of ASCII strings in each of a plurality of storage elements, wherein the plurality of ASCII strings represent a plurality of initial values of the serial circuit; and
storing one or more ASCII strings in each of one or more data structures wherein the one or more ASCII strings represent one or more mathematical operations in the serial circuit.

30. (Original) The apparatus as recited in Claim 29, wherein storing the one or more ASCII strings in each of one or more data structures comprises:
storing an ASCII string "XOR" for each addition operation the serial circuit; and

storing an ASCII string "AND" for each multiplication operation in the serial circuit.

31. (Original) The apparatus as recited in Claim 28, wherein simulating the serial circuit comprises:

executing the serial circuit for a plurality of cycles as required to produce one output represented by the plurality of parallel equations.

32. (Original) The apparatus as recited in Claim 27, the method further comprising:

synthesizing the hardware description language description implementation into a gate level implementation; and

manufacturing the ASIC from the gate level implementation.

33. (Original) The apparatus as recited in Claim 32, the method further comprising:

simulating the gate level implementation to verify accurate design implementation.

34. (Previously Presented) The apparatus as recited in Claim 27, wherein the complex polynomial equation is a Bose-Chaudhuri-Hocquenghem (BCH) code.

35. (Original) The apparatus as recited in Claim 27, wherein merging the one or more parallel equations into a hardware description language implementation of a Galois Field circuit comprises:

removing initial register values from each of the parallel equations; and

adding a feedback value to each of the parallel equations.

36. (Previously Presented) An apparatus for performing Galois field encoding comprising:

a transmit demultiplexer section module for receiving and aligning a plurality of SONET datastreams;

a Forward Error Correction (FEC) encoder coupled to the transmit demultiplexer section module, the FEC encoder for calculating and inserting FEC check bits into the plurality of SONET datastreams, wherein

the FEC encoder comprises a first circuit that implements one or more parallel equations, and

the one or more parallel equations are generated by simulating a serial circuit; and
a transmit line section module coupled to the FEC encoder, the transmit line section module for multiplexing the SONET data streams into a SONET signal.

37. (Original) The apparatus as recited in Claim 36, wherein the FEC encoder comprises:
a circuit representing a complex polynomial equation made by the method of:
producing one or more parallel equations in a hardware description language; and
merging the one or more parallel equations into a hardware description language implementation of a Galois Field circuit.

38. (Previously Presented) The apparatus as recited in Claim 37, wherein producing the one or more parallel equations comprises:
implementing the serial circuit representing the complex polynomial equation in a software program; and
simulating the serial circuit to produce the one or more parallel equations.

39. (Original) The apparatus as recited in Claim 38, wherein implementing the serial circuit comprises:
storing a plurality of ASCII strings in each of a plurality of storage elements, wherein the plurality of ASCII strings represent a plurality of initial values of the serial circuit; and
storing one or more ASCII strings in each of one or more data structures wherein the one or more ASCII strings represent one or more mathematical operations in the serial circuit.

40. (Original) The apparatus as recited in Claim 39, wherein storing the one or more ASCII strings in each of one or more data structures comprises:
storing an ASCII string "XOR" for each addition operation the serial circuit; and
storing an ASCII string "AND" for each multiplication operation in the serial circuit.

41. (Original) The apparatus as recited in Claim 38, wherein simulating the serial circuit comprises:

executing the serial circuit for a plurality of cycles as required to produce one output represented by the plurality of parallel equations.

42. (Original) The apparatus as recited in Claim 37, the method further comprising:
synthesizing the hardware description language description implementation into a gate level implementation; and
manufacturing the ASIC from the gate level implementation.

43. (Original) The apparatus as recited in Claim 42, the method further comprising:
simulating the gate level implementation to verify accurate design implementation.

44. (Previously Presented) The apparatus as recited in Claim 37, wherein the complex polynomial equation is a Bose-Chaudhuri-Hocquenghem (BCH) code.

45. (Original) The apparatus as recited in Claim 37, wherein merging the one or more parallel equations into a hardware description language implementation of a Galois Field circuit comprises:
removing initial register values from each of the parallel equations; and
adding a feedback value to each of the parallel equations.